

REMARKS

Claims 24-43 are pending in the present application. Claims 1-23 were previously cancelled. Claims 34-43 have been added, and claim 24 has been amended herein. No new matter has been added.

Claim 24 has been rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by U.S. Patent No. 5,903,035 to Wu et al. (hereinafter "Wu"). Claims 25-33 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Wu in view of U.S. Patent No. 5,668,035 to Fang et al. (hereinafter "Fang"). Applicants respectfully traverse these rejections.

Claim 24 has been amended to more clearly recite at least one of the distinguishing features of Applicants' invention. In particular, claim 24 has been amended to recite that "the logic gate oxide and the first doped polysilicon layer form a first transistor and the cell gate oxide, the first doped polysilicon layer, and the second polysilicon layer form a second transistor."

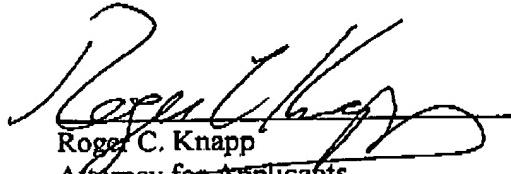
With regard to Wu, the reference relied upon by the Office Action in its rejection of claim 24, it is noted that Wu fails to disclose this feature. Rather, Wu assertedly discloses forming a self-aligned buried contact region in the substrate, not the formation of two different types of transistors.

Claims 25-33 depend from and further limit independent claim 24 in a patentable sense. Accordingly, Applicants respectfully request that the rejections of claims 25-33 be withdrawn as well.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the

address below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,



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